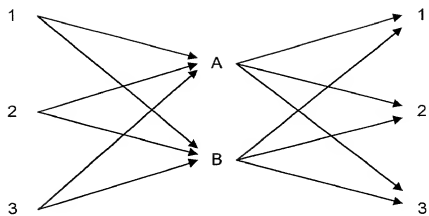


**FIGURE 1 (PRIOR ART)**



**FIGURE 2 (PRIOR ART)**

		Outputs		
		1	2	3
Inputs	1			
	2			
	3			

**FIGURE 3 (PRIOR ART)**

		Outputs		
		1	2	3
Inputs	1			A
	2			
	3			

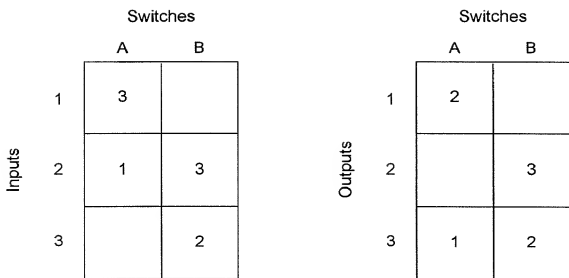
**FIGURE 4 (PRIOR ART)**

		Outputs		
		1	2	3
Inputs	1			A
	2	A		B
	3		B	

**FIGURE 5 (PRIOR ART)**

		Outputs		
		1	2	3
Inputs	1			$\frac{A}{B}$
	2	$\frac{A}{B}$		$\frac{B}{A}$
	3	A	B	

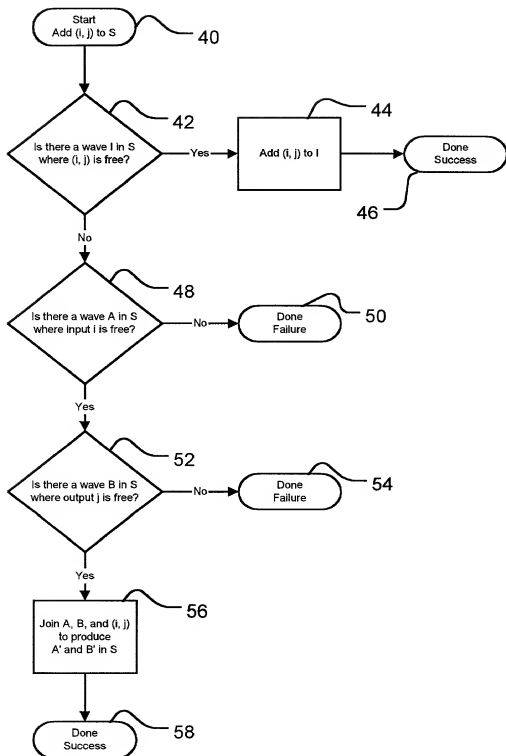
**FIGURE 6 (PRIOR ART)**



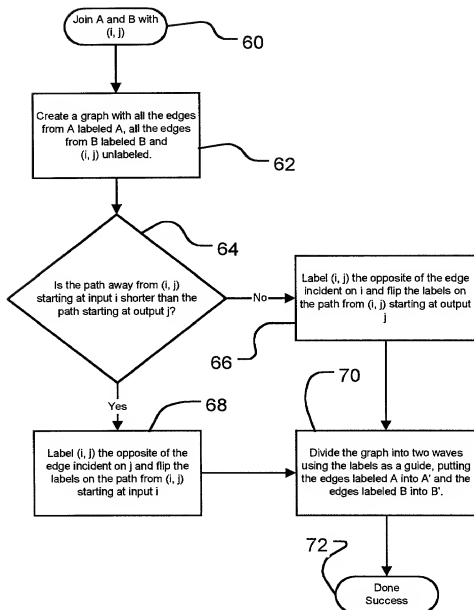
**FIGURE 7 (PRIOR ART)**



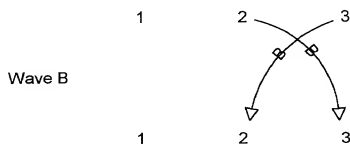
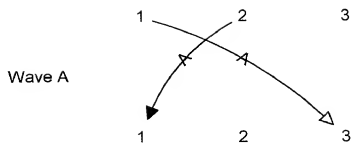
**FIGURE 8 (PRIOR ART)**



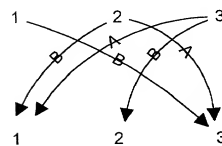
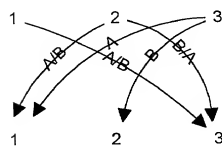
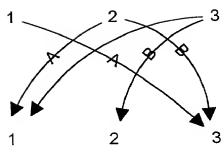
**FIGURE 9**



**FIGURE 10**

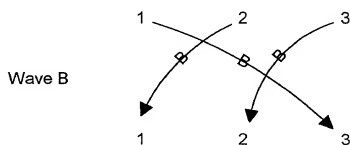
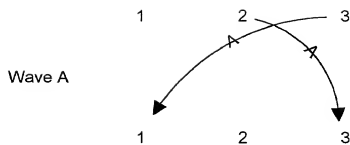


**FIGURE 11**



**FIGURE 12**



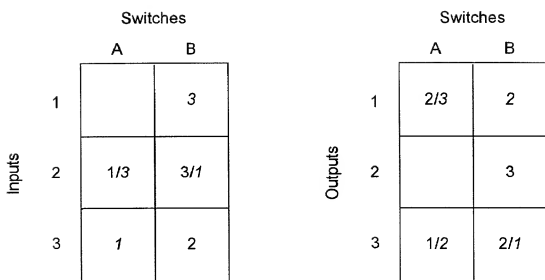


**FIGURE 13**

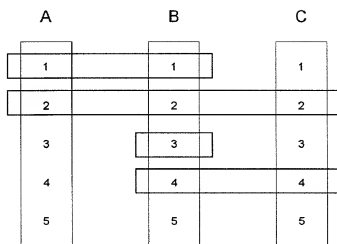
		Switches	
		A	B
Inputs	1	3	
	2	1	3
	3		2

		Switches	
		A	B
Outputs	1	2	
	2		3
	3	1	2

**FIGURE 14**



**FIGURE 15**



**FIGURE 16**